UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,664	10/23/2003	Alexander E. Andreev	03-1496	9953

24319 7590 08/09/2006

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106
MILPITAS, CA 95035

EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,664	ANDREEV ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-21* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed on May 15th, 2006, with respect to independent claims 1 and 7 have been considered but are not persuasive.

Applicant argues that the Prior Art of Record (Fujisawa) does not teach "providing a first single port memory module for an even address of an operation and providing a second single port memory module for an odd address of an operation". However, Fujisawa discloses switching the read and write clocks of the two FIFO line memories depending on whether the line address is either and odd or even number. This has the effect of providing one FIFO line memory for the even line address and while the other FIFO line memory is being provided for the odd line address (see Col. 15, lines 39-62). Therefore, Fujisawa does teach "providing a first single port memory module for an even address of an operation and providing a second single port memory module for an odd address of an operation".

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujisawa (5,086,346).

Regarding Claim 1, Fujisawa discloses a method for allowing a FIFO memory with single port memory modules (63, 63, Figure 15) to perform simultaneous read and write operations, comprising: providing a first single port memory module for an even address of an operation; providing a second single port memory module for an odd address of said operation (switch read clocks and write clocks of the two FIFO line memories depending on whether the line address is either odd or even... Col. 15, lines 39-62); alternating said even address and said odd address (alternating the use of line memories 62 and 63); and when both a read request and a write request reach one of said first single port memory module and said second single port memory module at a first clock cycle, fulfilling said read request at said first clock cycle and fulfilling said write request at a second clock cycle immediately following said first clock cycle (area signals are written using the write clock to the line memory 63 and at the same time, using the read clock, the area data from the line memory 62 is output...).

Regarding Claim 2, Fujisawa discloses the method wherein said operation is selected from a group consisting of reading and writing (alternating read and write operations between FIFO memories 62 and 63, Col. 15, lines 39-62).

Regarding Claim 3, Fujisawa discloses the method wherein said first single port memory module and said second single port memory module are identical (FIFOs 62 and 63) and are of half capacity (they are of half capacity since ins using them together as disclosed, they are doubling the storage area available, Col. 15, lines 39-62).

Claim 7 is rejected using the same rationale as that of Claim 1.

Claim 8 is rejected using the same rationale as that of Claim 2.

Claim 9 is rejected using the same rationale as that of Claim 3.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-6 and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa (5,086,346) in view of Microsoft Computer Dictionary.

Regarding Claim 4, Fujisawa discloses the method as disclosed in Claim 1. Fujisawa does not teach said first single port memory module and said second single port memory module being RAMs (random access memories). Microsoft Computer Dictionary discloses semiconductor based RAM memories that can be read and written to by hardware devices (Page 372). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memories of Fujisawa to be RAM memories since these can be read as well as written to and accessed in any order, thus facilitating multiple access operations.

Regarding Claim 5, Fujisawa discloses the method as disclosed in Claim 1. Fujisawa does not teach said first single port memory module and said second single port memory module being SRAMs (static random access memories). Microsoft Computer Dictionary discloses semiconductor based SRAM memories based on logic flip-flops that can hold information as long as there is enough power to run the device (Page 423). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memories of Fujisawa to be SRAM memories since they are fast memories.

Regarding Claim 6, Fujisawa discloses the method as disclosed in Claim 1. Fujisawa does not teach said first single port memory module and said second single port memory module being DRAMs (dynamic random access memories). Microsoft Computer Dictionary discloses semiconductor based DRAM memories that store information in integrated circuits containing capacitors (Page 159). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the memories of Fujisawa to be DRAM memories since these memories are simpler and hold more capacity.

Claim 10 is rejected using the same rationale as that of Claim 4.

Claim 11 is rejected using the same rationale as that of Claim 5.

Claim 12 is rejected using the same rationale as that of Claim 6.

Allowable Subject Matter

6. Claims 13-21 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of independent Claim 13 do not appear to be found in the Prior Art of Record.

Regarding Claim 13, Fujisawa discloses A FIFO memory with single port memory modules (Figure 15, 62, 63) for allowing simultaneous read and write operations, comprising: a first single port memory module for an even address of an operation; a second single port memory module for an odd address of said operation (switch read clocks and write clocks of the two FIFO line memories depending on whether the line address is either odd or even... Col. 15, lines 39-62), wherein said even address and said odd address alternate (alternating the use of line

memories 62 and 63); a memory control module, communicatively coupled to said first single port memory module and said second single port memory module, for controlling distribution of reading and writing requests between said even address and said odd address and performance of postponed writing (Demultiplexers 60 and 61, Figure 15); a data output selection module, communicatively coupled to said first single port memory module and said second single port memory module, for selecting a value between a first output value from said first single port memory module and a second output value from said second single port memory module and holding said value until a next read request comes (data selector 64, Figure 15).

Fujisawa does not teach nor suggest in the claimed combination a read and write request update module, communicatively coupled to said memory control module and said data output selection module, for updating RE (read enable) and WE (write enable) input flags to avoid reading from empty said first single port memory module and said second single port memory module and writing into full said first single port memory module and said second single port memory module; and an address and status update module, communicatively coupled to said read and write request update module, said memory control module and said data output selection module, for updating values of address registers R_ADR (read address) and W_ADR (write address) used for access to said first single port memory module and said second single port memory module.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

July 31, 2006

Midys Rojas
Examiner
Art Unit 2185

MR

Mano Padmanabhan 8/4/06
SUPERVISORY PATENT EXAMINER